

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	82	(wire with load with model)	USPAT	OR	OFF	2004/12/22 13:31
L2	32525	(bi adj directional)	USPAT	OR	OFF	2004/12/22 13:32
L3	553	L2 with wire	USPAT	OR	OFF	2004/12/22 13:34
L4	539	(703/14.ccls. 703/17.ccls. 703/19.ccls.) and model	USPAT	OR	OFF	2004/12/22 13:36
L6	751	(703/14.ccls. 703/17.ccls. 703/19.ccls.)	USPAT	OR	OFF	2004/12/22 13:36
L7	11	L1 and L6	USPAT	OR	OFF	2004/12/22 13:37

11

- L1 (Simulat\$ or emulat\$) with (bidirectional or two way inout or duplex) near (Wire or line)
- L2 L1 Same (Port or node) same (Path or loop or mesh)
- L3 L2 same (control\$ or detect\$) same (change or v.
- L4 L1 same (VHDL or Verilog hardware des
- L1 L4 and vital timing